

REMARKS

This amendment is submitted together with a Request for Continued Examination, in response to the Final Office Action mailed June 28, 2005.

Support for the claim amendments can be found in the Specification as filed, paragraphs [0010], [0014], [0018], and Figs. 2 and 3, for example. Accordingly, no new matter has been added.

Claim 1 has been amended to more particularly point out that the memory testing engine is embedded in the bus controller to have a memory interface, which is shared with the memory testing engine (for accessing the random access memory). In addition, claim 1 has also been amended to clarify that where the memory testing engine uses data, address and control pathways that are also used by the bus controller, this is so that if data traffic from the processor is being passed to a memory module by the bus controller, the testing engine cannot run a test function. Support for these amendments can be found in the Specification as filed, in Figs. 2 and 3, and paragraphs [0014] and [0018] (where in Fig. 2 data traffic originates from the CPU 211, and Fig. 3 showing an example MTE embedded in a bus slave controller). Accordingly, no new matter has been added.

Miner does not teach or suggest Applicants' system as it appears in amended claim 1, because in Miner, there is no memory testing engine that executes test operations on the random access memory and is embedded in a bus controller to have a memory interface shared with the memory testing engine. The Final Office Action refers to test execution logic 560 as teaching Applicants' claimed *memory testing engine*, while test management logic 570 is indicated as being the claimed *bus controller*. Applicants' claimed *bus* is interpreted by the Examiner as reading on the test control bus 575, in contrast to the normal bus 554. This analogy to Miner fails to anticipate Applicants' claim 1 as amended here, because Miner does not teach or suggest that element 560 is embedded in element 570 to have a memory interface which is shared. Indeed, the two elements are connected by a bus 574 and as such are not deemed *embedded within one another*.

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It should also be noted that in Miner, there is no teaching or suggestion that memory 510 is to be accessed with *data traffic* as opposed to *test functions*, via test control bus 575. The latter appears only to be used for configuring the test management logic 570 and not to *pass data traffic directly to the memories*. That is why the local bus 532 is controlled by a separate bus unit 530 which is used to pass data traffic to the memory 510 from a separate, normal bus 554 (during the normal mode of operation of the microprocessor). Accordingly, it would not have been obvious to modify this design of Miner so as to teach or suggest Applicants' claimed system.

As to claim 2, the Final Office Action on page 11 holds that although Miner does not explicitly teach a second memory test engine, it would have been obvious to duplicate the teaching of Miner to include additional test execution logic and test management logic entities to perform a similar function. However, Applicants' claim 2 is not merely duplicating the random access memory, memory testing engine, and second bus controller. Rather, claim 2 refers to the second bus controller *connected to the processor by the bus*. In other words, the first and second bus controllers are connected to the same bus. That topology is not taught or suggested by merely duplicating the bus unit 530, test management logic 570, and test execution logic 560 of Miner. That is because those elements are in a single microprocessor 501 which has a test control bus 575 that connects it to a test controller 580. There is no teaching or suggestion that the test control bus 575 be coupled to multiple test management logic units 570. If anything, Miner appears to suggest that additional memory 510 could be tested by simply expanding the capability of the test execution logic 560 (via the local bus 532 and control bus 564). As an alternative, multiple microprocessors 504 may be tested in parallel by the test controller 580, but that would require that the test management logic 570 in each additional microprocessor be connected to its separate test control bus 575. Accordingly, Applicants' claim 2, which recites additional memory testing engines and additional bus controllers that are connected to the processor by the same bus, would not have been obvious from Miner.

As to claim 16, Applicants continue to disagree with the rejection of this claim as being anticipated, because Miner does not teach or suggest that a processor transmits a number of initiation signals via **the same bus**, to multiple memory testing engines via

multiple bus controllers, respectively. In Miner, the test management logic 570 of each microprocessor is initialized over the microprocessor's respective test control bus 575. There is no teaching or suggestion that multiple memory test engines be added that are accessed **over the same test control bus**. If anything, multiple microprocessors may be tested in parallel by the test controller, but over separate test control buses. Note how Miner makes a clear distinction between the test control bus and the normal bus used by the microprocessor. Accordingly, one of ordinary skill in the art would not be motivated to modify the testing operations of Miner in the manner required by Applicants' claim 16.

As to claim 18, this claim has been amended to refer to the additional operation of transmitting data traffic from the processor through the same bus used for configuring the memory test engine, to one of the random access memories. This occurs via the memory data, address and control pathways, while such are under control of the respective bus controller. Miner does not suggest transmitting any *data traffic* from the test controller through the test control bus to the random access memories being tested, because the actions of the test controller are limited to configuring the test management logic 570. Any non-test functions (*data traffic*) are performed through the normal bus 554, not the control bus 575. Accordingly, it would not have been obvious to modify Miner to arrive at the capability recited in Applicants' claim 18 as amended here.

Turning now to claim 30, Applicants continue to disagree with the rejection of claim 30 as being anticipated by Miner, because Miner is directed to a single, microprocessor in which there is integrated memory and test management logic. There is no teaching or suggestion that the memory being tested in Miner is associated with an application specific integrated circuit (ASIC). Although it may be common practice to incorporate memory into a more complex, ASIC, Miner does not disclose any such teaching. It is well known in the art that a microprocessor is quite different than an ASIC. an ASIC is a custom integrated circuit, whereas a microprocessor, such as the one disclosed in Miner is a general purpose device. Moreover, Miner does not teach or suggest that the memory testing engine be embedded in a utility bus slave (UBS) controller that is on the ASIC. Note that support for this amendment to claim 30 can be

found in the Specification as filed, paragraph [0010] (“The embodiments circumvent the time and efficiency problems inherent in testing by moving the testing procedure from a centralized testing system that must individually test each of the RAMs associated with ASICs to a memory testing engine (MTE) embedded on or coupled with the bus slave controller on each integrated circuit. This allows the testing to be performed on each RAM at once, reducing the time cost of testing each individual RAM. Additionally, by embedding the MTE in the bus slave controller, the equipment needed to test the machine can be reduced, increasing both fiscal and spatial efficiency.”).

Miner does not teach or suggest that a memory testing engine be embedded in the UBS controller on an ASIC. Note that the term “utility bus” refers to a type of back plane bus used in electronics cabinets, to receive circuit cards (such as in a server or other scalable piece of electronics). The understanding of those skilled in the art is supported by the attached printouts of web pages from two different sources, namely Cisco BPX 8600 Series Switches, Installation, Part 2 (see for example pages 5 and 6 of 8), and whatis.techtarget.com definition of VMEbus, on pages 1 and 2 of 3 in the enclosed printouts. The test control bus in Miner does not teach or suggest that the test management logic 570 is a utility bus slave controller or equivalent. Rather, the test control bus 575 is simply a dedicated, limited duty test bus that appears to be a point-to-point connection from the microprocessor 501 to a test controller 580. There is no suggestion of implementing a *utility bus controller* (as understood by those skilled in the art) in the microprocessor 501 of Miner, to interface with that test control bus 575.

Turning now to claim 44, Applicants respectfully disagree with the Examiner’s overly broad interpretation of the means plus function limitations in claim 44 as reading on the single microprocessor and test controller environment of Miner. Nevertheless, Applicants have rewritten claim 44 to cover a different embodiment of the invention. Claim 44 now recites an apparatus having means for controlling a bus, where means for testing memory is embedded in the bus controlling means to share the same memory interface. There is also means for initiating the testing by accessing the testing means over the same bus. Finally, there is means for disabling the testing means while passing data traffic from the initiating means to the memory over the same bus. Miner does not teach or suggest such an apparatus.

Any dependent claims not mentioned above are submitted as being neither anticipated nor obvious, for at least the same reasons given above in support of their base claims.

If necessary, the Commissioner is hereby authorized in this, concurrent and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2666 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17, particularly, extension of time fees.

Respectfully submitted,
BLAKELY, SOKOLOFF, TAYLOR, & ZAFMAN LLP

Dated: October 28, 2005

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Margaux Rodriguez October 28, 2005



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Safety Requirements

The following paragraphs contain general safety information.

For safe operation, observe the following:

- Only authorized personnel should be allowed access to the IPX.
- To ensure safe and proper operation of the IPX (together with peripheral equipment), use only the power cords, cables, and connectors specified for the attached peripheral equipment, and make sure they are in good condition.

Power and Grounding

1. Ensure that the IPX frame is attached to an isolated ground connection (frame attached directly to ground through an uninterrupted line).
2. As part of the branch circuit that supplies the unit, install a grounding conductor that is identical in size to the ground and ungrounded branch circuit supply conductors. This grounding conductor is green with yellow stripes.
3. Make sure that all attached plug receptacles in the vicinity of the unit or system are of a grounding type, and the grounding conductors serving these receptacles are connected to earth at the service equipment.

CEPT Requirements

Consider the CEPT requirements prior to connecting a private network to the public switched networks in certain international service areas, as follows:

Step 1 Only those 48 VDC power sources that comply with EN60950 can connect to the 48 VDC power distribution unit.

Step 2 The following port types on the IPX are approved to carry public-switched non-voice traffic (OTR001, issue 3, port types 2DN):

- BC-E1 ports (G.703, 2048 Kbits per second).
- SDI-RS-232, LDI-RS-232, BC-SR, SDI-RS-449, FRI-V.35 (approved for direct connection to V.35 leased digital circuit).

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 [Installation, Part 2](#)

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- SDI-RS-449 (when connected via StrataCom RS449/X.21 interface cable).

Step 3 The following port type on the IPX is approved to carry PSTN voice traffic:

- BC-E1 ports (G.703 2048 Kbps, when connected to the CDP and NTC front cards).

Note Each cable must be attached so that its removal requires the use of tools.

Step 4 To keep end-to-end delays at 10 ms or less, adhere to the following configuration constraints in relation to the IPX:

- Only d-type connections may be used.
- Routes must not exceed one hop.
- Trunk queue depths must be modified. If an IPX System Administrator cannot do this, contact StrataCom ISC.

EMI Requirements

Compliance with Emission requirements depends upon adherence to the installation steps in this manual, including installation of faceplates for all slots and the use of shielded cables between systems.

Parts Checklist

Before proceeding, go through the parts checklists that follow to verify that all ordered parts are present and in good condition. If anything is missing or damaged, report it to your StrataCom Order Administration representative.

IPX Cabinets

Check the cabinet for the following:

- _____ [IPX 16/32] The unit has the correct number of shelves (1 or 2).
- _____ The unit has the correct power supply type (AC or DC). For IPX 16/32: open the back door. For IPX 8: look on the back. The words "AC (or DC) PWR DISTRIBUTION" are on the back panel of the Power Distribution Unit.
- _____ The unit has the correct number of power supplies (1, 2, 3, or 4).

Plug-In Cards

Verify that all cards are present for the ordered configuration.

- | | |
|--------------------------------|--------------------------------|
| _____ Correct number of NPCs | _____ Correct number of LDIs |
| _____ Correct number of SCCs | _____ Correct number of BC-T1s |
| _____ Correct number of SCC-Bs | _____ Correct number of BC-E1s |
| _____ Correct number of CDPs | _____ Correct number of BC-SRs |
| _____ Correct number of NTCs | _____ Correct number of BC-J1s |
| _____ Correct number of FRPs | _____ Correct number of BC-Y1s |

_____ Correct number of FRIs	_____ Correct number of LECs ¹
_____ Correct number of SDPs	_____ Correct number of AITS
_____ Correct number of SDIs	_____ Correct number of BC-AIT-T3s
_____ Correct number of LDPs	_____ Correct number of BC-AIT-E3s
_____ Blank covers for all unused back slots	_____

¹Used in IPX 32 nodes only.

Note An inventory list of the installed cards is taped to the IPX cabinet. The list includes each card's serial number, revision number, and slot number. Serial and revision numbers are also found on the component side of each card. After accounting for all cards, tape the inventory inside the back cover of this manual for future reference.

Installing the IPX Cards

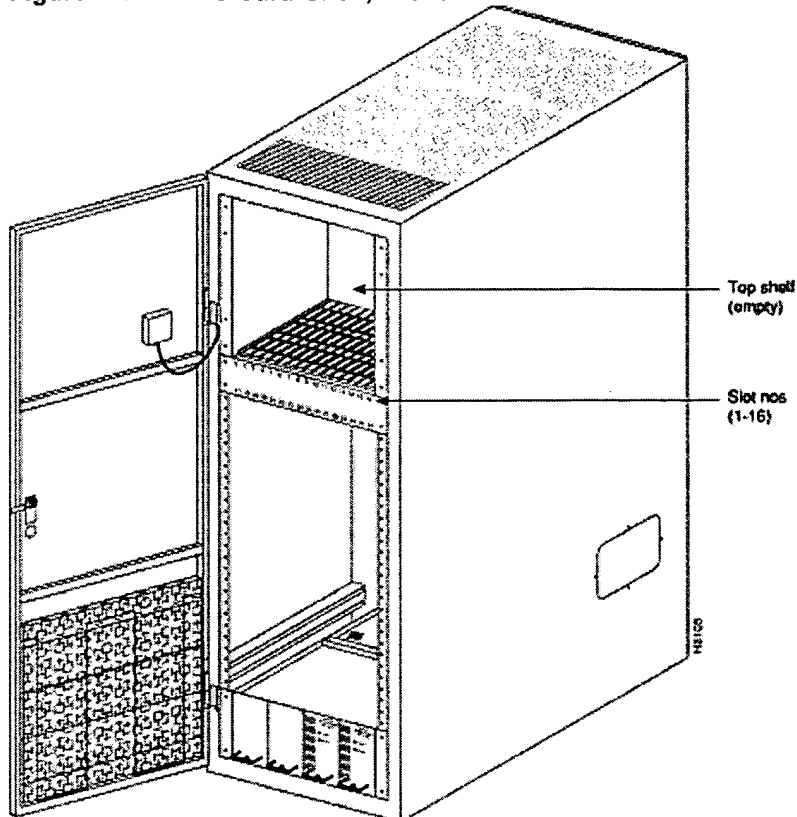
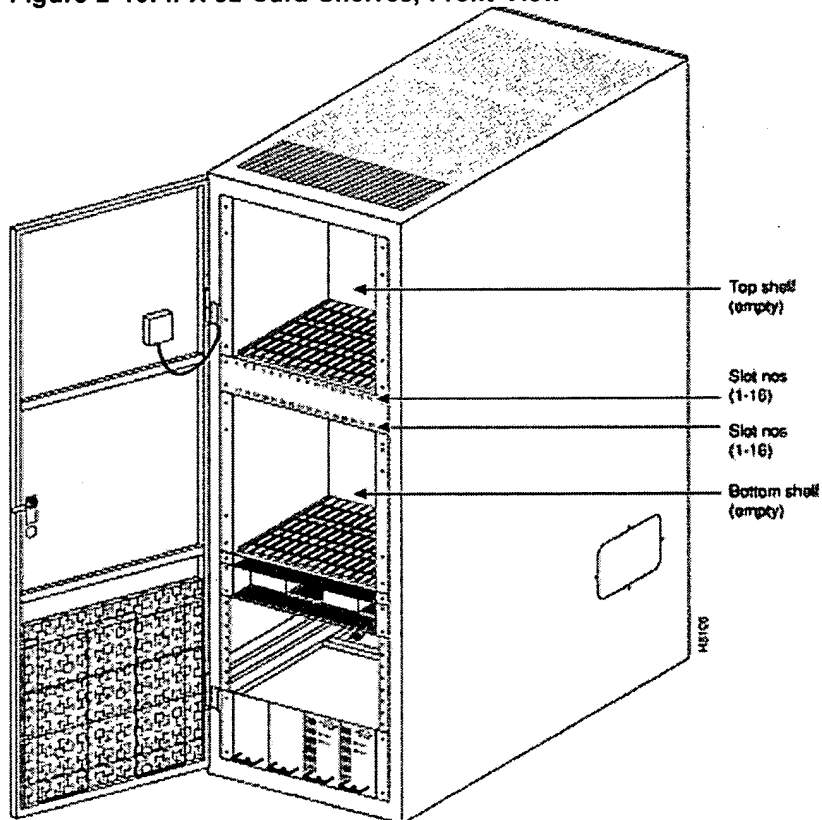


Caution Ground yourself before handling IPX cards by placing a wrist strap on your wrist and clipping the strap lead to the cabinet, or use the wrist strap that is connected to the cabinet.

The IPX 16 has one (upper) card shelf. Its card slot numbers are 1 through 16 (left to right when viewed from the front of the cabinet). In addition to an upper card shelf, the IPX 32 contains a bottom shelf with card slots numbered 17 through 32. A front view of the IPX 16 and the IPX 32 appear in [Figure 2-9](#) and [Figure 2-10](#), respectively.

The locations of the system cards in an IPX depend on the configuration. The only cards that are always in the same locations are the NPCs, the SCC, and the LEC. The locations of these cards for an IPX 16 and an IPX 32 are as follows:

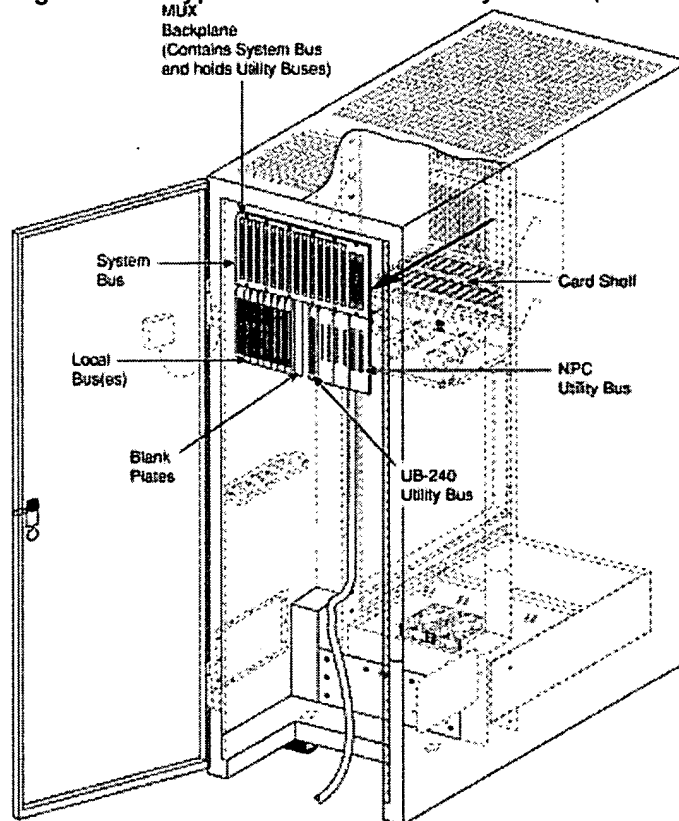
- IPX 16 (Non-Redundant)
 - NPC: front slot number 1
 - SCC: back slot number 1 behind PCC in front slot number 1
- IPX 16 (Redundant)
 - NPCs: front slot numbers 1 and 2
 - SCC: back slot number 1 behind PCC in front slot number 1
- IPX 32 (Non-Redundant)
 - NPC: front slot number 1
 - SCC: back slot number 1 behind NPC front slot number 1
 - LEC: back slot number 17
- IPX 32 (Redundant)
 - NPC: front slot number 1
 - SCC: back slot number 1 behind NPC front slot number 1
 - NPC: always in front slot number 17
 - LEC: back slot number 17 behind NPC front slot number 17

Figure 2-9: IPX 16 Card Shelf, Front View**Figure 2-10: IPX 32 Card Shelves, Front View**

Use of the remaining slots depends on the node configuration. The position of the

various utility buses installed on the System Bus backplane determines in which slots the cards can be installed. Figure 2-11 shows the six types of utility buses as viewed from the back of the cabinet. These are the NPC-UB, LB/1, and UB 240 utility buses. Except for the NPC bus, the locations of these buses can vary from node to node.

Figure 2-11: Typical Locations of Utility Buses (Rear View)



The use of the MUX backplane, system bus, and utility buses is as follows:

- MUXBUS Backplane
 - 16-slot backplane that provides power to all cards contains the system bus and any installed utility buses. Each card shelf has one MUXBUS backplane.
- NPC Utility Bus
 - The IPX uses two different types of NPC utility buses: a one-slot bus and a two-slot bus.
 - In an IPX 16, the two-slot bus is installed in slot 1 and supports two NPC front cards and extends the I/O interface of the NPCs to an SCC installed in back slot 1.
 - In an IPX 32, a one-slot bus is installed in both slot 1 and slot 17 and supports an active and a standby NPC. The SCC installed in back slot 1 is connected by cabling to an LEC installed in back slot 17, thereby extending the system bus to the lower shelf (slots 17 through 32).
- Local Utility Bus (LB/1)
- provides a single-slot bus for the following:
 - CDP in the front slot, with a BC-T1, BC-J1, or BC-E1 in the back slot behind the CDP card.
 - NTC in the front slot, with a BC-T1, BC-Y1, BC-SR, or BC-E1 in the

back slot behind the NTC.

- LDP in the front slot, with a four-port or eight-port LDI in the back slot behind the LDP.
- UB-240 Utility Bus
 - Single-slot bus for an SDP in the front slot, with an SDI in the back slot behind the SDP card.

IPX 8 Card Shelf Configuration

The IPX 8 cabinet contains one card shelf with front and back slots for card access. Figure 2-12 illustrates the slot numbering.

Front slots 1 and 2 are reserved for the primary and redundant NPC controller cards. The accompanying SCC is factory-installed in rear slot 1. If the system has a redundant PCC/NPC, it resides in front slot 2, and rear slot 2 remains empty.

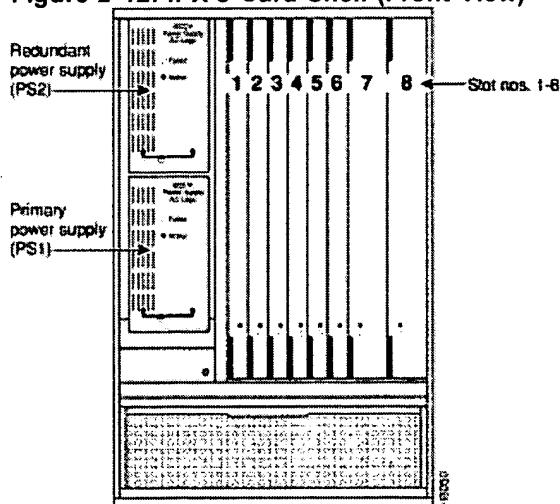
Various cards can reside in card slots other than 1 and 2. These include the NTC, CDP, FRP, SDP, LDP, ARC, and AIT. The cards in the back slots are the network and user interface cards. These include the BC-E1, BC-T1, BC-SR, FRI, SDI, ARI, ATM-T3/E3 and LDI. Most card types can reside anywhere a vacant slot and the appropriate utility bus exists. Only the controller card and power supply have assigned slots for primary and redundant units.

System assemblies indicated as T1 are configured with a BC-T1 as the back card associated with the NTC and CDP. Assemblies indicated as E1 are configured with a BC-E1 as the back card associated with the NTC and CDP. System assemblies indicated as J1 are configured with a BC-J1 as the back card associated with the NTC card and a BC-Y1 as the back card associated with the CDP.

Installing IPX 8 Plug-In Cards

The IPX 8 has one card shelf. The card slot numbers are 1 through 8 (left to right from the front of the cabinet). Figure 2-12 shows a front view of the card shelf. The locations of the system cards in an IPX depend on the configuration. The NPCs, and SCC occupy reserved card slots.

Figure 2-12: IPX 8 Card Shelf (Front View)



The locations for the NPCs, the SCC, and the power supplies are as follows:

- Single NPC configuration:
 - NPC: front slot number 1

- SCC: back slot number 1
- Redundant NPC configuration:
 - Primary NPC: front slot number 1
 - Redundant NPC: front slot number 2
 - SCC: back slot number 1
- Single Power Supply configuration:
 - Power Supply in lower left power supply slot
- Redundant Power Supply configuration:
 - Primary Power Supply number 1 in lower left power supply slot
 - Redundant Supply number 2 in upper left power supply slot

Installing a Redundant IPX 8 Power Supply

If a second power supply is later added for redundancy, it is used as a hot backup. Remove the front top blank panel and install it in the upper power supply slot in place of the blank panel (Figure 2-12).

Expansion into Empty Slots

Use of the remaining empty slots in the cabinet depends on the node configuration.

Each slot requires a utility bus to provide an electrical interface between the front card and the back card. You must not randomly install a card in an empty slot because the card may require a specific utility bus that may or may not be installed.

For the IPX 8, the choice of utility buses for the last several slots narrows down to either Local Bus 1 (LB/1) for the GDP, NTC, ANT, and LDP cards or the UB-240 bus for the SDP card.

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VMEbus

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A VMEbus system is based on the VME standard. The VME standard defines the mechanical specifications such as board dimensions, connector specifications, and enclosure characteristics, as well as the electronic specifications for sub-bus structures, signal functions, timing, signal voltage levels, and master/slave configurations. The most recent VME standard is the VME64 standard. The VME64 standard specifies a 64-bit data path for 6U cards, a 32-bit data path for 3U cards, twice the bandwidth for data transmission, lower noise, and Plug and Play features. Since the VME64 standard, an extension called the VME64x was added that supports hot swap. VME64 cards can be used on older VME bus systems and older VMEbus cards can be used on VME64 systems.

In 1997, a modified VME bus architecture called the VME320 was released by Arizona Digital. This architecture is designed to increase data transfer to 320 Mbps and bandwidth to 500 Mbps. The backplane design is different from the original VMEbus backplane.

The VMEbus system uses Eurocards. A Eurocard is a European designed circuit board that uses a 96-pin plug instead of an edge connector making it more durable. There are three sizes: 3U which is 4 x 6 inches, 6U which is 6 x 12 inches, and 9U which is 14 x 18 inches. 3U cards support 8- and 16-bit data paths and 6U cards support 32-bit data paths. The VME standard does not support 9U cards. Each card is plugged into a backplane. A backplane can have up to 21 slots for cards. A VMEbus system is scalable and modular, which means a card can be added when needed without having to make any other changes to the system.

A real-time operating system (RTOS) is included when a VMEbus system is purchased. An RTOS is better for VMEbus systems because of their ability to do a task within a certain time limit. Non real-time operating systems can be used but are not recommended.

A VMEbus system uses a master/slave architecture. A master is a device that controls another device. For example, a computer sends data to a printer. The computer is the master, and the printer is the slave because the printer cannot control the computer. A VMEbus system may have several master devices, which is why it is called a multiprocessing bus.

A VMEbus system has four sub-buses: the arbitration bus, the data transfer bus, the priority interrupt bus, and the utility bus.

- The arbitration bus controls the requests from various devices using an arbiter module. It gives permission to each device to use the bus and notifies requesting devices when the bus is busy. Requests are based on priority. Requests that are the same in priority are daisy-chained. The arbiter module resides in slot 1 of the backplane.
- The data transfer bus is used for reading and writing operations between modules.
- The priority interrupt bus handles interrupts and monitors the interrupt request lines, which range from interrupt request 1 to IRQ7. IRQ7 has the highest priority.
- **The utility bus supports a system clock.**

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